Remarks

Claims 1 to 21 remain pending.

The Examiner rejected claims 1 to 21 under 35 USC 112, first paragraph, on the basis that the claimed subject matter is not described in the specification.

Applicants respectfully disagree, and submit that the subject matter of the claims is fully supported and explained in the specification as originally filed, at least in the paragraphs identified below.

The Examiner provides an exemplary discussion of claim 1 in the Office Action.

For the Examiner's convenience, independent claim 1 is provided below:

> *A method for managing latency comprising:*
>
> *receiving data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources;*
>
> *providing a provisioning bit for each output; and*
>
> *synchronizing high-order and low-order outputs by adjusting a pointer for the low-order sources based on the provisioning bit.*

The Examiner states that "it is unclear whether the claimed invention receives both SDH and SONET frames", and that "the Examiner could not find support for such feature in the specification" (see the Office Action at page 2). However, Applicants respectfully submit that the original specification clearly states that the network can be a SONET and/or SDH network. Specifically, page 4 line 30 to page 5 line 1 recite (emphasis added):

> *….the network can be a synchronous optical network (SONET) and/or synchronous digital hierarchy (SDH) network.*

Accordingly, since the network can be a SONET network and/or an SDH network, the apparatus as claimed in claim 1 is capable of receiving both SONET and/or SDH frames.

Applicants also respectfully point to page 2 lines 5 to 14 of the application, which disclose:

> *The method includes receiving data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-*

> *order tributary unit (TU) and virtual tributary (VT) sources, providing a provisioning bit for each output associated with a memory, and adjusting a pointer for the low-order (VT/TU) sources based on the provisioning bit such that the high-order (STS/STM/AU-5/AU-3) and low-order (VT/TU) outputs are synchronized.*

Furthermore, page 5 lines 19 to 21 recite:

> *It will be understood however that the invention applies to equivalent SDH, and other, structures and apparatus (e.g. TU switching and TU alignment).*

With regard to the manner in which high order and low order outputs are synchronized, page 8 lines 1 to 5 disclose by way of example that:

> *…. to ensure STS and VT frames arrive together, the frames supplied to the switch that are to be switched at the VT level have their payload advanced by a predetermined number of clock cycles to compensate for the delays associated with VT switching etc. This is achieved by adjusting the high order pointer values (e.g. the AU-4 pointers in SDH or the STS-1 pointers in SONET) to relocate the position of the low order pointers (e.g. the TU pointers or VT pointers).*

Accordingly, Applicants respectfully submit that the subject matter claimed in independent claims 1, 11, and 19 is fully described in the specification in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, to make and use the same as required under 35 USC 112, first paragraph. Claims 2 to 10, 12 to 18, 20 and 21 recite additional features which are also fully described in the original specification.

Therefore, withdrawal of the rejection under 35 USC 112, first paragraph, is respectfully requested.

No fee is believed due for this submission. However, Applicant authorizes the Commissioner to debit any required fee from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP. The Commissioner is further authorized to debit any additional amount required, and to credit any overpayment to the above-noted deposit account.

Respectfully submitted,

JARABEK, Andrew et al.

By: /Curtis B. Behmann/

Curtis B. Behmann
Reg. No. 52,523
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1100
Ottawa, ON K1P 1J9
CANADA
Tel: (613) 237-5160
Fax: (613) 787-3558
E-mail: ipinfo@blgcanada.com

CBB/IT/cf